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21 Techniques and modules for element specification in a time - delay logic simulator

John L. Fike, S. A. Szygenda

June 1973 **Proceedings of the 1st symposium on Simulation of computer systems**

Publisher: IEEE Press

Full text available: pdf(872.73 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the development of element models (basic gates and flip-flops) for use in a multi-modal, assignable-delay logic simulator known as TEGAS2. The basic mechanism of this event-driven simulator is first described, together with the operation of the three basic simulation modes (nominal-delay two-value simulation, nominal-delay three-value simulation, and three-value simulation using an ambiguity region to provide race and hazard detection). The criteria used in d ...

22 A complete interactive simulation environment GPSS/360-Norden

Julian Reitman, Donald Ingerman, Jerry Katzke, Jon Shapiro, Kenneth Simon, Burton Smith

December 1970 **Proceedings of the fourth annual conference on Applications of simulation**

Publisher: Winter Simulation Conference

Full text available: pdf(760.68 KB) Additional Information: full citation, abstract, references

Norden's expanded and interactive version of GPSS/360 has been extensively improved through new data entry and storage capabilities, a new report generator, selective output display, and HELP blocks to enable model manipulation and to provide a "window" to view the simulation during its progress. The data entry and manipulation system allows the user to input and display matrix savevalues through an IBM 2250 Display Unit. Titles may be placed on rows and columns to si ...

23 Load balancing: Cycle stealing under immediate dispatch task assignment

Mor Harchol-Balter, Cuihong Li, Takayuki Osogami, Alan Scheller-Wolf, Mark S. Squillante

June 2003 **Proceedings of the fifteenth annual ACM symposium on Parallel algorithms and architectures**

Publisher: ACM Press

Full text available: pdf(334.39 KB) Additional Information: full citation, abstract, references, citings, index terms

We consider the practical problem of task assignment in a server farm, where each arriving job is immediately dispatched to a server in the farm. We look at the benefit of cycle stealing at the point of the dispatcher, where jobs normally destined for one

machine may be routed to a different machine if it is idle. The analysis uses a technique which we refer to as dimensionality reduction via busy period transitions. Our analysis is approximate, but can be made as close to exact as desired, and ...

Keywords: cycle stealing, distributed system, load sharing, matrix analytic methods, server farm, starvation, supercomputing, task assignment, unfairness

24 Ensemble: a graphical user interface development system for the design and use of interactive toolkits

M. K. Powers

November 1989 **Proceedings of the 2nd annual ACM SIGGRAPH symposium on User interface software and technology**

Publisher: ACM Press

Full text available: pdf(1.67 MB) Additional Information: full citation, abstract, references, index terms

User Interface Development Systems (UIDS), as opposed to User Interface Management Systems or UI Toolkits focus on supporting the design and implementation of the user interface. This paper describes Ensemble, an experimental UIDS that begins to explore the electronic creation of interaction techniques as well as the corresponding design processes. Issues related to the impact on the components of the development system are discussed. Finally, problems with the current implementation and fu ...

25 Applications of spatial simulation of discrete entities: Statistical properties of the simulated time horizon in conservative parallel discrete-event simulations

G. Korniss, M. A. Novotny, A. K. Kolakowska, H. Guclu

March 2002 **Proceedings of the 2002 ACM symposium on Applied computing**

Publisher: ACM Press

Full text available: pdf(678.47 KB) Additional Information: full citation, abstract, references, index terms

We investigate the universal characteristics of the simulated time horizon of the basic conservative parallel algorithm when implemented on *regular lattices.* This technique [1, 2] is generically applicable to various physical, biological, or chemical systems where the underlying dynamics is asynchronous. Employing direct simulations, and using standard tools and the concept of *dynamic scaling* from non-equilibrium surface/interface physics, we identify the universality class of the ...

Keywords: Monte Carlo, conservative parallel discrete-event simulation, non-equilibrium surface growth, scalability, stochastic processes

26 Optimistic simulation I: Pal: a new fossil collector for time warp

Voon-Yee Vee, Wen-Jing Hsu

May 2002 **Proceedings of the sixteenth workshop on Parallel and distributed simulation**

Publisher: IEEE Computer Society

Full text available: pdf(664.42 KB) Publisher Site Additional Information: full citation, abstract, references

Fossil collection plays an important role in managing the memory utilization in parallel simulations with Time Warp. We describe a novel fossil collection method that incurs low overhead in reclaiming memory buffers occupied by processed events. The time complexities of the existing and the proposed methods are analyzed and presented. We have also tested the methods with a number of real-world and synthetic workload simulations, and confirmed that the proposed method indeed incurs lower overhead ...

Keywords: fossil collection, memory management, optimistic methods, time warp

27 Multithreading and value prediction: Handling long-latency loads in a simultaneous multithreading processor

Dean M. Tullsen, Jeffery A. Brown

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available: pdf(1.17 MB) Publisher Site Additional Information: full citation, abstract, references, citings

Simultaneous multithreading architectures have been defined previously with fully shared execution resources. When one thread in such an architecture experiences a very long-latency operation, such as a load miss, the thread will eventually stall, potentially holding resources which other threads could be using to make forward progress.This paper shows that in many cases it is better to free the resources associated with a stalled thread rather than keep that thread ready to immediately begin ex ...

28 Improving fine-grained irregular shared-memory benchmarks by data reordering

Y. Charlie Hu, Alan Cox, Willy Zwaenepoel

November 2000 **Proceedings of the 2000 ACM/IEEE conference on Supercomputing (CDROM)**

Publisher: IEEE Computer Society

Full text available: pdf(422.50 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We demonstrate that data reordering can substantially improve the performance of fine-grained irregular shared-memory benchmarks, on both hardware and software shared-memory systems. In particular, we evaluate two distinct data reordering techniques that seek to co-locate in memory objects in close proximity in the physical system modeled by the computation. The effects of these techniques are increased spatial locality and reduced false sharing. We evaluate the effectiveness ...

29 Hybrid simulation models of computer systems

H. D. Schwetman

September 1978 **Communications of the ACM**, Volume 21 Issue 9

Publisher: ACM Press

Full text available: pdf(558.15 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the structure and operation of a hybrid simulation model in which both discrete-event simulation and analytic techniques are combined to produce efficient yet accurate system models. In an example based on a simple hypothetical computer system, discrete-event simulation is used to model the arrival and activation of jobs, and a central-server queueing network models the use of system processors. The accuracy and efficiency of the hybrid technique are demonstrated by com ...

Keywords: central server model, performance evaluation, queueing network models, simulation

30 Issues in the pragmatics of qualitative modeling: lessons learned from a xerographics project

Jeff Shrager, Daniel S. Jordan, Thomas P. Moran, Gregor Kiczales, Daniel M. Russell

December 1987 **Communications of the ACM**, Volume 30 Issue 12

Publisher: ACM Press

Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The photocopier is one of the most complex machines because xerography involves many types of physical phenomena. ARIA is a qualitative simulation of xerography that is intended to teach technicians the reasons behind some of the subtle problems that occur in copiers. This effort to model xerography exposed shortcomings in the techniques of qualitative modeling as applied to complex systems and helped to better understand the impact of certain basic modeling decisions.

31 Highlights of CMU research on CAD, CAM and CAT of VLSI circuits

John Paul Shen

November 1986 **Proceedings of 1986 ACM Fall joint computer conference**

Publisher: IEEE Computer Society Press

Full text available: pdf(1.35 MB) Additional Information: full citation, references, index terms

32 Design of a joint operations planning simulator

James R. Jansen, Mark A. Roth

December 1987 **Proceedings of the 19th conference on Winter simulation**

Publisher: ACM Press

Full text available: pdf(682.39 KB) Additional Information: full citation, abstract, references, index terms

The Joint Operations Planning System (JOPS) is a Department of Defense system for the conduct of the joint planning process. We describe the design of microcomputer implementation of a JOPS simulator, called JPLAN. We present some background on JOPS and JPLAN, problems with the current simulation, and our approach for a new microcomputer implementation which eliminates the "user hostile" interface for users and maintainers of the simulation.

33 Improving digital circuit simulation: a knowledge based approach

John A. Benavides, Dana L. Wyatt

December 1988 **Proceedings of the 20th conference on Winter simulation**

Publisher: ACM Press

Full text available: pdf(843.58 KB) Additional Information: full citation, abstract, references, citings, index terms

The simulation of digital logic circuits is a common practice in design automation. Because of advances in integrated circuit technology, currently available digital circuit simulator can not model all circuit behavior. Combining artificial intelligence and simulation techniques, a knowledge based simulator was designed and constructed to model non-standard circuit behavior. Circuit designer expertise on behavioral phenomena is used to diagnose, analyze, and emulate this behavior in the

34 DATAPATH: a CMOS data path silicon assembler

Tom Marshburn, Ivy Lui, Rick Brown, Dan Cheung, Gary Lum, Peter Cheng

July 1986 **Proceedings of the 23rd ACM/IEEE conference on Design automation**

Publisher: IEEE Press

Full text available: pdf(898.11 KB) Additional Information: full citation, abstract, references, citings, index terms

As an integration of automatic silicon assembly and simulation tools, the DATAPATH Silicon Assembler produces mask geometries and netlists from input specifications written in a Hardware Description Language, MADL. DATAPATH consists of a library of data path cells (i.e. registers, bus prechargers, drivers, interconnects, ALU's and other logic

elements) in a flexible bus architecture. The cells are highly parameterized and procedurally described in a hierarchical manner. The layout is automa ...

35 Performance evaluation of FMOSSIM, a concurrent switch-level fault simulator

Randal E. Bryant, Michael Dd. Schuster
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**
Publisher: ACM Press

Full text available: pdf(560.16 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents measurements obtained while performing fault simulations of MOS circuits modeled at the switch level. In this model the transistor structure of the circuit is represented explicitly as a network of charge storage nodes connected by bidirectional transistor switches. Since the logic model of the simulator closely matches the actual structure of MOS circuits, such faults as stuck-open and closed transistors as well as short and open-circuited wires can be simulated. By usi ...

36 Structured models and dynamic systems analysis: the integration of the IDEF0/IDEF3 modeling methods and discrete event simulation

Larry Whitman, Brian Huff, Adrien Presley
December 1997 **Proceedings of the 29th conference on Winter simulation**
Publisher: ACM Press

Full text available: pdf(779.21 KB) Additional Information: full citation, references, citings, index terms

37 Simulation of multiple time-pressured agents

Scott D. Anderson
December 1997 **Proceedings of the 29th conference on Winter simulation**
Publisher: ACM Press

Full text available: pdf(902.67 KB) Additional Information: full citation, references, citings, index terms

38 Using VRML to access manufacturing data

Sandy Ressler, Qiming Wang, Scott Bodarky, Charles Sheppard, Gregory Seidman
February 1997 **Proceedings of the second symposium on Virtual reality modeling language**
Publisher: ACM Press

Full text available: pdf(843.69 KB) Additional Information: full citation, references, citings, index terms

Keywords: data access, manufacturing environment, user interfaces, virtualf environments

39 A comparative study of parallel algorithms for simulating continuous time Markov chains

David M. Nicol, Philip Heidelberger
October 1995 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 5 Issue 4
Publisher: ACM Press

Full text available: pdf(2.21 MB) Additional Information: full citation, abstract, references, citings, index terms

This article describes methods for simulating continuous time Markov chain models, using

parallel architectures. The basis of our method is the technique of uniformization; within this framework there are a number of options concerning optimism and aggregation. We describe four different variations, paying particular attention to an adaptive method that optimistically assumes upper bounds on the rate at which one processor affects another in simulation time, and recovers fr ...

Keywords: Markov chains

40 Optimization of a corn-processing simulation model

David Humphrey, Julius Chu
December 1992 **Proceedings of the 24th conference on Winter simulation**
Publisher: ACM Press
Full text available: pdf(624.41 KB) Additional Information: full citation, references, index terms

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